Practical Sessions 11–13

ADVANCED SYSTEMS WITH TIMS

You will cover one topic in each of these three weeks. If the number of students is not too large, you will all do Session 11 in Week 11 and so on. However, if numbers rise unexpectedly, we will not have enough equipment, and the Sessions will be done in a different order for different groups.

There will not be printed practical notes along the normal lines, rather you will mostly work from 'Ideas for Experiments' compiled by the TIMS manufacturer. It is considered that this will normally be a good three hours' work, and you may well have to be selective.

Handouts provided (for the session only) in the laboratory include these instructions, specifications for all modules used, and often reading from sources other than Schwartz. Some extra notes for each session are provided below.

Your report need not contain copies of large slabs of the printed instructions,
provided that you make it quite clear what you did by direct references to those notes.

As usual, make sure that your report makes all possible qualitative and quantitative comparisons of experimental results with theory.

Practical Session 11
BIT ERROR RATES

The effect of limited bandwidth and added noise on the transmission of data.
Eye patterns as visual indicators; choosing a decision level.
Bit error rate as a function of SNR.

Reading: Lecture Notes 19, 26, F2; Schwartz 181–182, 408–410, 422–432 .
Extra reading may be found in the laboratory handout.

TIMS AMSI User Manual: 6-11, 22-24.

TIMS AMSI Ideas for Experiments: 5-13 (reference only).

After examining waveforms and eye patterns for a variety of channel characteristics, you study how the Decision Maker works. This allows you to make measurements of the bit error rate as a function of SNR and compare this with the theory. These measurements must take account of the delays, inversions and level shifts needed to ensure that the Decision Maker works correctly, and that the final output is fairly compared with the original data.

Notes on how to make these measurements are given below, and need to be followed to the letter if the results are to be valid.

Bit Error Rate as function of SNR etc.

Set up these units, from left to right;

1. Audio Oscillator
   Set Δf to give 2 kHz.

2. Sequence Generator
   Set switches for minimum sequence length (both up).

3. Tuneable LPF
   Initially set Tune clockwise, Gain top centre, Wide.

4. Baseband Channel Filters
   Initially set to 1.

5. Noise Generator
   Initially set to 0 dB.

6. Adder
   Initially set G and g to top centre.

7. Wideband True RMS Meter
   Initially set to AC 10 V.

8. Decision Maker
   Set to NRZ-L, INT.

9. Utilities

10. Error Counting Utilities
    Check the PCB switches – they should be in the default positions as follows:

J1		NORM	
Active Level	Trig	HI	⎫ SW1
	Gate	LO	⎭
Count Mult		×1	SW2

11. Twin Pulse Generator
    Initially set Width to min., Delay to max..

12. Twin Pulse Generator
    As for 11.

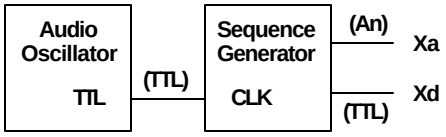
Note that the Procedure that follows tells you how to get sensible results.

It does not tell you everything you should do and observe and record.

Think of useful and informative things to do and record at each stage so that your report will clearly illustrate how the TIMS units worked, how results agree with theory, how you understand the circuit behaviour, and so on.

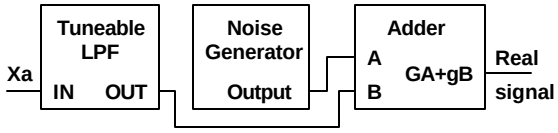
Procedure

1. Set up a random bit sequence clocked at 2 kHz.



   Trigger the CRO (ch. 3, 5V with ×10 probe) off the SYNC output of the Sequence Generator for most of the time (except for eye patterns). Check that some pulses of the output are only 0·5 msec. wide, and note that Xa and Xd are the inverse of each other (as well as having different levels).

2. Set up a sequence which simulates the result of using a real channel, i.e. limited frequency response and added noise.

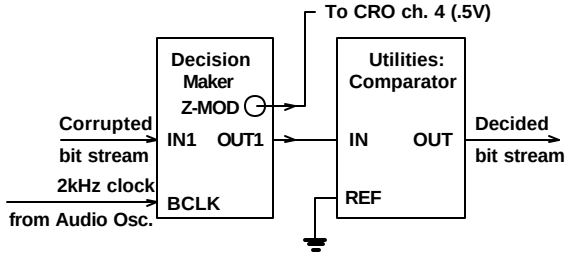


   Set g with G=0 so that the output swings ±2 V. Now set G with +20 dB of noise so that the noise swings about ±2 V about the signal.

3. Refine these settings using the True RMS Meter.
   Disconnect the noise from the Adder.
   Adjust g to give an indicated Adder output of 2·00 VRMS.
   Disconnect the bit stream from the Adder and connect the noise (+20 dB).
   Adjust G to give an indicated Adder output of 1·41 VRMS.
   Retain these G and g settings.
   With both Adder inputs connected, measure the RMS output voltage; does it agree with a value predicted from the separate signal voltages?
   (Some students get close to the correct answer by adding the two voltages and dividing the sum by the square root of 2, but this is nonsense.
   For example, what if one of the signals were zero?)
   Turn the noise down to 0 dB.

4. Now try to square up the bit stream using the Decision Maker.
   Note that we used the analogue bit stream for two reasons:
   - It is an inverted version of the digital bit stream, but this compensates for inversion in the Adder.
   - When set to NRZ-L, the Decision Maker has a threshold at 0 V, central on the waveform.

   However, the bit stream out of the Decision Maker is bipolar, so it needs to be set to TTL levels for later use.

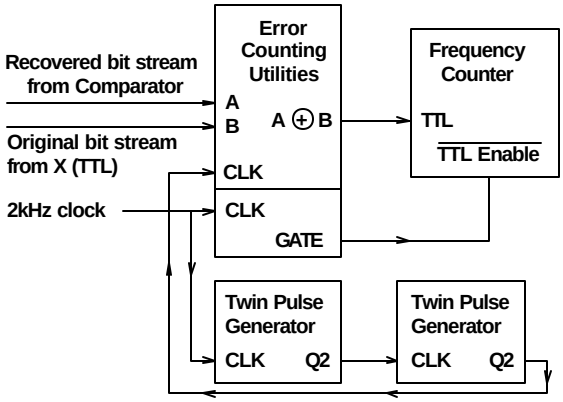


   Observe IN1, OUT1, Z-MOD on the CRO, while still triggering off the SYNC of the Sequence generator (ch. 3).
   The short pulses of Z-MOD indicate the times at which the output level is changed, depending on whether the input is then positive or negative.
   The decision should not be made while the input is changing, so adjust the Decision Point until Z-MOD pulses avoid such transitions
   but coincide with the centre of the shortest input pulses.
   Check that the output is now a good copy of the input; note however that the output has to be a delayed version of the input.
   You may like to try other filters;
   set the Tuneable LPF to its widest setting and put this signal also through the Baseband Channel Filters.
   (N.B.: 2 & 4 are swapped.)

5. Check the operation of the Decision Maker using eye patterns; simply trigger the CRO off the 2kHz clock instead of SYNC for the purpose.
   Reduce the channel bandwidth and note the deterioration in shape of the bit stream; note also that its delay also varies, so that the Decision Point needs to be varied for best results.
   Add more noise to the bit stream and note that the safe vertical eye height is reduced – in fact with 22 dB of noise the eye closes with the recommended settings.

6. Observe the behaviour of the Decision Maker on a longer timebase, observing the original (X - TTL) bit stream and the recovered bit stream while again triggering off the SYNC of the Sequence Generator. Check that some Decision Point settings produce errors in the output.

7. Use the Error Counting Utilities to count such errors.



Start with a bit stream near perfect, using the widest LPF setting and 0 dB of noise. Initially disconnect Q2 from the CLK input of the Error Counting Utilities. Observe A, B, A⊕B and note that, although one bit stream is a good copy of the other if the Decision Point is reasonable, the exclusive-OR indicates lots of errors because of their relative delay.

Observe A⊕B and the Q2 output of the second Twin Pulse Generator. With both delays at a maximum and a reasonable (if not optimum) setting of the Decision Point, the Q2 pulses should only occur when A⊕B is LOW.

This means that the Q2 pulses occur when the original and recovered waveforms are equal; however, if the Decision Maker was in error a Q2 pulse would occur when A⊕B=1.

Connect the Q2 pulse to the CLK input of the Error Counting Utilities. You should now only get pulses from A⊕B when an error really occurs.

Provided that you can keep the adjustments so that there is a time when the original and recovered waveforms are equal, and can adjust the Q2 timing to get sampling pulses then, you are in a position to make real bit-error-rate measurements.

8. Measure the bit error rate as a function of SNR.

Put the LPF to its widest setting; the Decision Point is then not too critical. Ensure, as above, that you are ready to measure real errors due to noise.

Monitor A⊕B and increase the noise (2dB steps) until you start to see only an occasional error on the CRO. Start with the noise 2 dB lower.

Check that the signal alone is 2·00 VRMS.

Set the Pulse Counter section of the Error Counting Utilities to $\times 10^5$; one measurement will therefore take about 50 seconds.

The measurement routine is:

- Check and record the signal in VRMS, by disconnecting the noise from the Adder.
- Similarly measure the noise signal in VRMS.
- Reset the Frequency Counter (set on COUNTS) (red button).
- First check that the clock is at 2 kHz (using the CRO). Press the red TRIG button of the Pulse Counter of the Error Counting Utilities to start the 10^5-pulse gate (about 50 sec.) and start counting.
  (Notes: Ignore the first pulse; it is spurious. An 'Active' light indicates that the count is proceeding. One simple check is to disconnect the A input to the ex-OR; this should give 50000 errors.)

Now measure the bit error rate as a function of SNR for successive 2dB increases in noise level.

Compare with theory.

Practical Session 12
LINE CODES

Study of various line codes for favourable properties such as: easy extraction of clock, minimal spectral width, no dc component, immunity to inversion, error detection capability.

Reading: Lecture Notes 20; Couch 144–163; Roden 208–213; Schwartz 192, 355 .
Extra reading may be found in the laboratory handout.

TIMS AMSI User Manual: 25-31.

TIMS AMSI Ideas for Experiments: 14-16.

Record the waveforms for the various line codes for the full 32 bits of data in the sequence.
This will be easier if you use the ×10 timebase scale and decalibrate it so that the transitions of the waveforms occur on main graticules of the CRO screen; some will occur with a half-division delay.

A good scheme is to use the back of ordinary graph paper for the waveforms; put your sheet on something white so that the grid lines are easily visible.

Make sure that you check each waveform against the stated method of generating it. It would be best to have a record in your report of what these methods are.

When you try the inverted codes, explain your results; don't just state what they are.

Try AC coupling using a series 47nF capacitor, not the nonsense method given in the Ideas. Explain these results also.

Practical Session 13
DELTA MODULATION

Variation of step size and clock rate – effect on overload noise and quantisation noise. Study of various methods of modulation and demodulation.

Reading: Lecture Notes 17; Schwartz 145–159 .

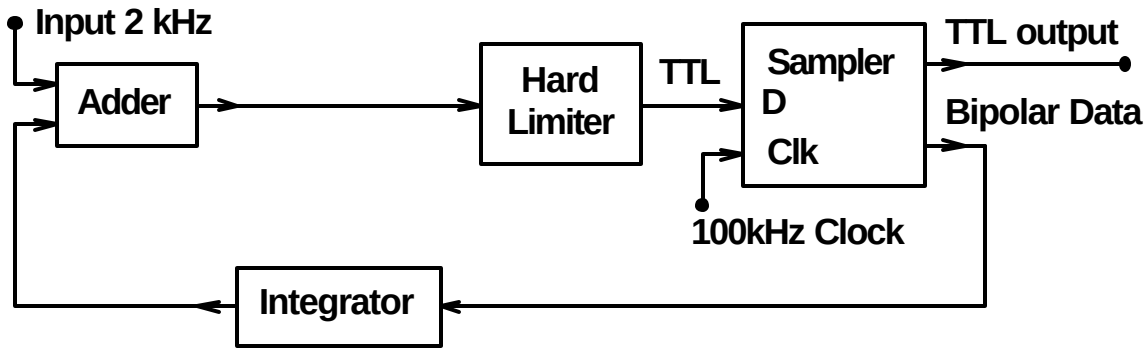
TIMS AMSI User Manual: 12-21.

TIMS AMSI Ideas for Experiments: 19-29.

It is unlikely that you will get through all of the tests suggested in the Ideas, but do as much as you can. A reasonable scheme is to go through sections 6.1, 7.1, 7.2, 6.2, 7.2, 6.3, 7.1 in that order, testing demodulation for each modulator.

The modulators and demodulators given as Ideas do not correspond exactly to those in your printed notes, so a few brief notes follow.

6.1 Simple Delta Modulator



This samples at well above the Nyquist rate.

Note that the circuit forms a feedback loop, comparing the integral of the bipolar data output with the input (in the adder, which produces an error signal). The loop attempts to make the two inputs to the adder equal (and opposite).

If the input is zero, the output will alternate rapidly, with equal times for a HIGH and a LOW value, so that the output of the integrator is zero, equal to the input.

If the input now suddenly changes to a positive value, the bipolar data output will jump to a constant state which opposes the change at the adder, and will stay there until the integrator output reaches the new input value; the output will then revert to a 50% duty cycle and the integrator will hold the new input voltage.

Note that any dc input will give the same output − a 50% duty cycle.

If the input is a ramp of voltage, the output will take on a duty cycle corresponding to that average voltage which, applied to the integrator, tracks the ramp; the faster the ramp, the higher the average voltage.

What is sent is therefore the rate of change of the input; after integration in the Delta Modulator it tracks the input voltage. The demodulation process will need to perform integration on the transmitted data stream, but the result will have an arbitrary dc level.

Note again that what is compared with the input (in the adder) is the integral of the bipolar output, which should therefore be the differential of the input.

Overload noise can occur if the output is a constant 2 V (or -2 V); the resulting slope of the ramp from the integrator is the maximum slope of the input before overload occurs.

So much for the principle of this delta modulator. But what about the step size; how is it determined?

A basic integrator produces an output v_{out} from an input v_{in} according to

$$v_{out} = -\frac{1}{t}\int v_{in}\,dt$$

where $t = RC$ is the time constant of the R and C used in the circuit.
If the integrator has had an input of ±2 V (from the bipolar signal) for time T_S, the output will change (between sample instants) by

$$\frac{\pm 2T_S}{t}$$

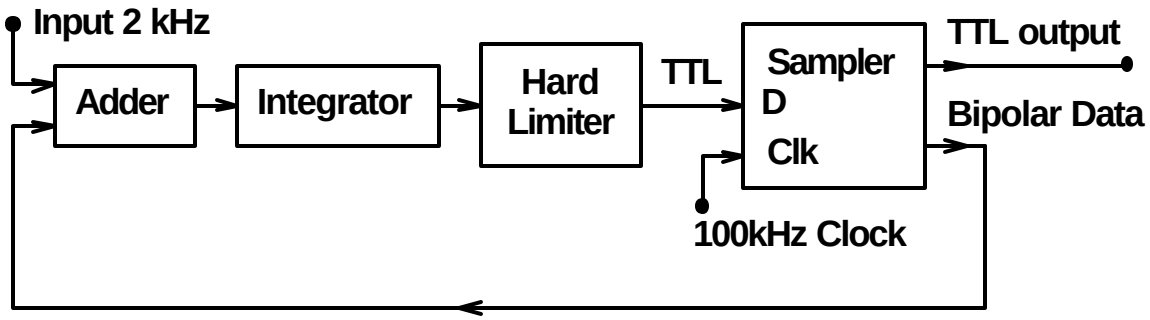
and this is clearly the step size.

The TIMS integrator has three possible values of R, giving three step sizes to choose from.

It also has three possible clock frequencies; note that increasing the time of integration also increases the step size.

In the first laboratory circuit there is an added complication − the adder has adjustable gain from each input to the output. In order to avoid overload when first it is tested, you should probably set appreciably higher gain from the integrator input than from the signal input. (As a rough guide, set the integrator gain control fully clockwise, and the message gain control about half-way.) The output should not spend appreciable time at a steady high or low voltage, but should rapidly alternate most of the time; the integrator output should not have long straight sections but should be quite jagged. This adjustment may be refined later if necessary.

6.2 Delta-Sigma Modulator



Here the integrator is moved from its previous position; the error is integrated rather than the output. (However, the error is an analogue voltage, and is not digitised.)

Note that what is compared with the input (in the adder) is the bipolar output, so that we could expect the output to represent the input directly, not its rate of change.

For a given dc input voltage, the output should alternate rapidly between HIGH and LOW, with the duty cycle adjusting so that the average voltage is equal to the input voltage. The adder output swings rapidly between two equal and opposite voltages, so that the integrator output ramps above and below the dc input voltage; the average error is zero and the output alternates rapidly between HIGH and LOW.

The demodulator need only average the bipolar data, and the frequency response reaches right down to dc.

Note that both an RC circuit and an integrator can be regarded as low-pass filters for the demodulator. However, an integrator has a $1/f$ frequency response, which an RC circuit only has beyond the cutoff frequency.